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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/930,365	08/15/2001	Masahiro Takeuchi	15.45/6059	3437

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EXAMINER

VU, QUANG D

ART UNIT PAPER NUMBER

2811

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/930,365

Applicant(s)

TAKEUCHI, MASAHIRO

Examiner

Quang D Vu

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on amendment filed on 06/17/03.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 20-26 and 32-59 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 20-26 and 32-59 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: |

DETAILED ACTION

Claim Objections

1. Claim 38 is objected to because of the following informalities: In line 2, the phrase “forming an polishing stopper layer...” should be changed to “forming a polishing stopper layer...”. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 20-25, 32-34, 38-39, 40-49 and 51-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,087,243 to Wang.

Wang teaches the first layer (11) comprises an epitaxial growth layer (see figures 1a-f; column 6, lines 14-18).

Regarding claim 21, Wang teaches removing the polishing stopper layer (13) after planarizing the dielectric layer (16) (column 6, lines 44-54).

Regarding claim 22, Wang teaches an oxidizing at least a portion of the first layer in the at least one trench prior to forming the dielectric layer in and above the trench (see figures 1a-b; column 6, lines 44-48).

Regarding claim 23, Wang teaches forming a pad layer (12) between the first layer (11) and the polishing stopper layer (13) (see figure 1a-c).

Regarding claim 24, Wang (figures 1A-H) teaches a method for manufacturing a semiconductor device including a trench isolation region, the method comprising:

- forming a first layer (11) on a semiconductor substrate;
- forming a polishing stopper layer (13) above the first layer;
- forming at least one trench (14) by etching the first layer while using the polishing stopper layer as a mask;
- forming a dielectric layer (16) in and above the trench; and
- planarizing the dielectric layer using the polishing stopper layer (13) as a stopper (see figures 1a-c; column 6, lines 44-50).
- removing the polishing stopper layer (13) after planarizing the dielectric layer (16) (column 6, lines 44-54);
- subjecting the dielectric layer to a thermal treatment at a temperature about 900° C to 1100° C after removing the polishing stopper layer (column 6, lines 44-60); and
- after the subjecting the dielectric layer to a thermal treatment at a temperature about 900° C to 1100° C, forming a well in the semiconductor substrate adjacent to the trench (column 6, lines 56-60).

Wang teaches subjecting the dielectric layer to a thermal treatment at a temperature about 900° C to 1100° C after removing the polishing stopper layer, which overlaps the temperature range of the claimed invention (column 6, lines 44 – 60). Wang differs from the claimed invention by not showing subjecting the dielectric layer to a thermal treatment at a temperature

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of least 1050° C after removing the polishing stopper layer. It would have been obvious to one having ordinary skill in the art at the time the invention was made for subjecting the dielectric layer to a thermal treatment at a temperature of at least 1050° C, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 25, Wang differs from the claimed invention by not showing the thermal treatment is carried out in an atmosphere comprising 0.1 volume % to 10 volume % oxygen. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to find the optimal concentration of oxygen in the atmosphere, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 32, Wang (figures 1A-H) teaches a method for manufacturing a semiconductor device, comprising:

providing a semiconductor layer (11);

forming a plurality of trenches (14) in the semiconductor layer (11);

forming a thermal oxide layer (15) on the semiconductor surface in the trenches (14)

(column 6, lines 44-46);

depositing a dielectric layer (16) into the trenches (14) and filling the trenches (14) with the dielectric layer (16);

thermally treating the dielectric layer (14) in the trenches at a temperature about 900° C to 1100° C; and

after the thermally treating the dielectric layer (16) in the trenches (14), forming a well (30, 31) region.

Wang differs from the claimed invention by not showing to form a well region between a first trench and a second trench of the plurality of trenches, wherein the first trench is adjacent to the second trench, and wherein the well region is formed to extend continuously in the semiconductor layer from the first trench to the second trench. One having ordinary skill in the art would have been required to form the well region that extends continuously in the semiconductor layer from the first trench to the second trench. It is known in the art as shown for example by US Patent No. 6,028,339 to Frenette et al. (figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the well region that extends continuously in the semiconductor layer from the first trench to the second trench, since it is a well-known method.

Regarding claim 33, Wang teaches the dielectric layer (16) is formed in direct contact with the thermal oxide layer (15) in the trenches (14).

Regarding claim 34, Wang differs from the claimed invention by not showing the dielectric layer is formed with a film density of at least 2.1 g/cm^3 . It would have been obvious to one having ordinary skill in the art at the time the invention was made for the dielectric layer is formed with a film density of at least 2.1 g/cm^3 , since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 38, Wang teaches forming a polishing stopper layer (13) on the semiconductor layer (11) prior to form the plurality of trenches (14);

forming openings in the polishing stopper layer (13) above the regions in the semiconductor layer (11) where the plurality of trenches (14) are to be formed;

forming the dielectric layer (16) in the openings and on the polishing stopper layer (13), planarizing the dielectric layer (16) using the polishing stopper layer (13) as a stop; and removing the polishing stopper layer (13) after planarizing the dielectric layer (16) and prior to the thermally treating the dielectric layer (column 6, lines 44-60).

Regarding claim 39, Wang teaches forming an oxide pad layer (12) on the semiconductor layer (11) prior to form the polishing stopper layer (13) (column 6, lines 13-27).

Regarding claim 40, the disclosures of Wang are discussed as applied to claims 21-25, 32-34 and 38-39 above.

Regarding claim 41, Wang teaches forming a pad layer (12) on the semiconductor layer (11) prior to form the polishing stopper layer (13), wherein the pad layer (12) is formed between and in direct contact with the semiconductor layer (11) and the polishing stopper layer (13) (column 6, lines 13-27).

Regarding claim 42, Wang teaches the opening in the polishing stopper layer (13) also extends through the pad layer (12).

Regarding claim 43, Wang differs from the claimed invention by not showing isotropically etching the pad layer and upper portions of the dielectric layer after the removing the polishing stopper layer and prior to the conducting the thermal treatment. It would have been obvious to one having ordinary skill in the art at the time the invention was made for isotropically etching the pad layer and the dielectric layer because it proceeds in all directions at the same rate.

Regarding claim 44, the disclosures of Wang are discussed as applied to claim 43 above. Wang further teaches etching exposes upper surfaces of the semiconductor layer (11).

Regarding claim 45, the disclosures of Wang are discussed as applied to claims 43-44 above. Wang further teaches an oxide layer (16) is formed on the exposed upper surfaces of the semiconductor layer (11) after the etching and prior to the forming a well in the semiconductor layer.

Regarding claim 46, Wang teaches the oxide layer (16) is formed prior to the conducting a thermal treatment of the dielectric layer (16).

Regarding claim 47, the disclosures of Wang are discussed as applied to claim 34.

Regarding claim 48, Wang teaches the temperature of the thermal treatment about 900° C to 1100° C (column 6, lines 44 – 60). Wang differs from the claimed invention by not showing the temperature of the thermal treatment is 1100° C or higher. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the temperature of the thermal treatment is 1100° C or higher, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 49, Wang teaches the temperature of the thermal treatment about 900° C to 1100° C (column 6, lines 44 – 60). Wang differs from the claimed invention by not showing the temperature of the thermal treatment is in the range 1050° C to 1250° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the temperature of the thermal treatment is in the range 1050° C to 1250° C, since it has been held

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that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 51, Wang teaches the trench (14) includes sidewall surfaces and a bottom surface, the method further comprising of thermally oxidizing the sidewall surfaces and the bottom surface of the trench to form a thermal oxide layer (15) (column 6, lines 44-45) thereon, wherein the dielectric layer (16) is formed in direct contact with the thermal oxide layer (15).

Regarding claim 52, Wang teaches the thermally oxidizing the sidewall surfaces and the bottom surface of the trench is carried out at a temperature about 900° C to 1100° C (column 6, lines 44 – 60). Wang differs from the claimed invention by not showing the thermally oxidizing the sidewall surfaces and the bottom surface of the trench is carried out at a temperature in the range of at 700° C to 1150° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the thermally oxidizing the sidewall surfaces and the bottom surface of the trench is carried out at a temperature in the range of at 700° C to 1150° C, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 53, the disclosures of Wang are discussed as applied to claim 52.

Regarding claim 54, Wang differs from the claimed invention by not showing the thermally oxidizing the sidewall surfaces and the bottom surface yields an oxidation layer having a thickness in the range of 10 nm to 100 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the thermally oxidizing the sidewall

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surfaces and the bottom surface yields an oxidation layer having a thickness in the range of 10 nm to 100 nm, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

In re Aller, 105 USPQ 233.

Regarding claim 55, Wang teaches the semiconductor layer (11) comprises an epitaxial growth layer formed on a semiconductor substrate (10).

Regarding claim 56, Wang differs from the claimed invention by not showing the trench is formed with a trench width of no greater than 0.35 micrometer. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the trench is formed with a trench width of no greater than 0.35 micrometer, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 57, the disclosures of Wang are discussed as applied to claims 20-25, 32-34, 40-49 and 51-56. Wang further teaches forming a patterned resist layer on the polishing stopper layer (13), the patterned resist layer including an open region exposing part of the polishing stopper layer (13) over a trench formation region; and using the patterned resist layer as a mask, etching through the open region and forming at least one trench (14) by etching through the exposed part of the polishing stopper layer (13) and the pad oxide layer (12) and into the semiconductor layer (11) (column 6, lines 26-43).

Regarding claim 58, Wang teaches after forming the at least one trench (14) and prior to form the dielectric layer (16), forming a thermal oxide layer (15) on the semiconductor substrate (10) in the at least one trench (14).

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Regarding claim 59, the disclosures of Wang are discussed as applied to claims 48, 49 and 53.

4. Claims 26, 35-37, 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang as applied to claims 20-25 and 32-34 above, and further in view of US Patent No. 6,165,854 to Wu.

Wang differs from the claimed invention by not showing the dielectric layer is formed using high density plasma chemical vapor deposition. However, Wu teaches the dielectric layer (14) is formed using high density plasma chemical vapor deposition (column 4, lines 28-31). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the high density plasma chemical vapor deposited dielectric layer of Wu into the method taught by Wang because it improves the dielectric property of the dielectric layer.

Regarding claim 35, the disclosures of Wang are discussed as applied to claim 26.

Regarding claim 36, Wang teaches the semiconductor layer (11) comprises an epitaxial growth layer formed on a semiconductor substrate (10).

Regarding claim 37, Wang and Wu differ from the claimed invention by not showing a method, wherein the epitaxial growth layer has a thickness of at least 2 micrometer. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the epitaxial growth layer has a thickness of at least 2 micrometer, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

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Regarding claim 50, the disclosures of Wang are discussed as applied to claims 26 and 35.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

qv
July 28, 2003

~~SHOUXIANG HU~~
PRIMARY EXAMINER